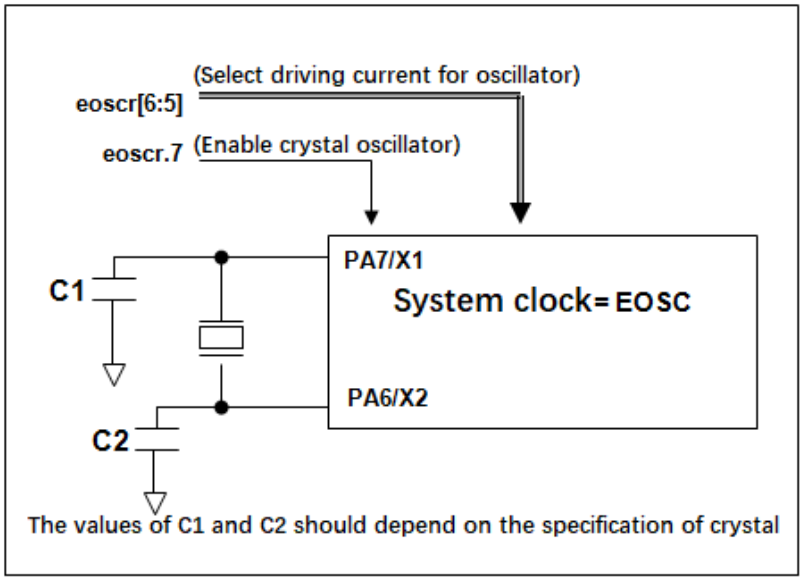
Application Notes When Using Crystal Oscillator

Applied for: All MCU with eosc

When using a single-chip microcomputer with Crystal Oscillator function, set the *eoscr* register according to the specification based on the selected Crystal Oscillator frequency. For example:

eoscr.[6:5]=01 : Low driving capability, for lower frequency, ex: 32KHz crystal oscillator
eoscr.[6:5]=10 : Middle driving capability, for middle frequency, ex: 1MHz crystal oscillator
eoscr.[6:5]=11 : High driving capability, for higher frequency, ex: 4MHz crystal oscillator

In general, low drive current can be selected to reduce power consumption under the following operating conditions. The recommended values of crystal capacitance C1 and C2 identified in the chip specification are only initial values, the user must adjust C1 and C2 capacitance according to the crystal manufacturer's suggested Load capacitance, operating voltage and other influencing factors to achieve optimal effect.



The capacitor values of C1 and C2 shall be adjusted to:

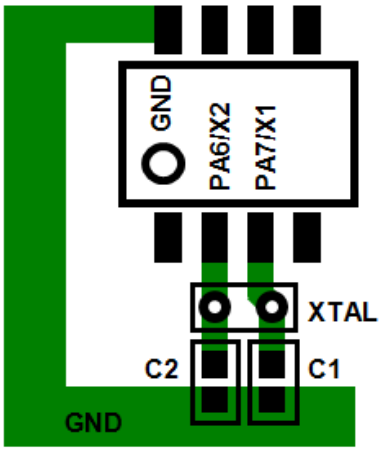
1. At Highest VDD and Lowest temperature, the PA6/X2 output waveform of crystal oscillator circuit must be a Clean Sine Wave. There can be no over driven phenomenon of chord wave being Clipped.
2. The crystal oscillator circuit must still operate normally under Highest Temperature and Lowest operating voltage (Lowest VDD), and the PA6/X2 sine wave cannot drive insufficient (the amplitude of sine wave is large enough).
3. Use C2 capacitor value greater than C1 capacitor value to improve the vibration.

When PA6/X2 output sine wave of crystal oscillator circuit exists the phenomenon of over driven, C2 can be increased to improve Over Driven, but it is not recommended to use capacitance value too far from the recommended value of crystal oscillator factory.

In order to ensure stable operation of the crystal oscillator on the designed circuit, pay attention to the following items when laying out the wiring on the PCB circuit board:

1. Oscillation circuit components (crystal oscillator, load capacitance) should be arranged next to the I/O pins (PA7/X1, PA6/X2 in the figure above) of the single chip microcomputer, as close as possible.
2. Connect the MCU I/O pins (PA7/X1, PA6/X2 in the figure above) and the PCB layout of crystal oscillator should be the shortest and not cross.
3. Configure GND at the bottom of the crystal oscillator.
4. Crystal oscillator and MCU I/O pin (PA7/X1, PA6/X2) contact to the ground resistance must have good insulation impedance, especially in 32.768K crystal oscillator application, because of its small operating current, such as reduced resistance to the ground, easy to have leakage to the ground, resulting in slow or no vibration phenomenon.

If the above matters are not paid attention to in the design, various faults such as vibration failure, unstable oscillation and inaccurate frequency will be caused. The following figure is a PCB layout example:



Since the operational stability and accuracy of the crystal oscillator circuit are affected not only by the above PCB layout and wiring, but also by the crystal oscillator, peripheral resistors and capacitors used. The user is required to provide a circuit board sample in normal operation, and request the crystal oscillator supplier to perform Oscillation Circuit Loop Analysis on the crystal oscillation circuit designed on the circuit board, In order to know whether the matching of the crystal oscillator in the entire oscillation line is good. If the matching is not good, the

oscillation frequency is not accurate, no vibration, oscillation instability and other phenomena will occur.

General crystal oscillator supplier's Oscillation Circuit Loop Analysis report contains the following three test items:

1. Measurement of Frequency Tolerance:

This project measures the overall error (PPM) of the crystal oscillation circuit on the circuit board under test, If the error is too large, the load capacitance value of crystal oscillator will be adjusted to improve the error, as shown in the following table:

C1/C2(pF)	F/on board(Hz)	F/on board(ppm)	F/xtal(ppm)	On board Dev.(ppm)
22/22	32769690	51.57	13.96	37.61
27/27	32768519	15.84	13.96	1.88

C1/C2(pF)：Represents the value of the crystal load capacitance used on the board, in pF
F/on board(Hz)：Represents the oscillation frequency of the crystal oscillation circuit, in Hz
F/on borad(ppm)：Represents the overall error of the crystal oscillation circuit, in ppm
F/xtal(ppm)：Represents the error of the crystal monomer, in ppm

On board Dev.(ppm)：Represents the deviation between the overall error of crystal oscillation circuit and the error of crystal oscillator. The load capacitance of the crystal oscillator is generally adjusted to improve this offset to minimize the impact of the oscillating circuit on the crystal oscillator error (for example, stray capacitance on the circuit board) and to ensure that the overall crystal oscillator error is as close to the crystal oscillator error specification as possible.

For example, in the table above, the oscillation circuit was originally designed to use a 22pF load capacitor. The overall error of the oscillation circuit is 51.57ppm, the crystal monomer error is 13.96ppm(within the crystal oscillator error specification +-20ppm), and the error offset is 37.61ppm. After adjusting the load capacitance to 27pF, the error deviation can be reduced to 1.88ppm, that is, for the crystal oscillator with an error specification of +-20ppm, the overall error of the oscillation circuit can be controlled within 21.88ppm ~ -18.12ppm.

2. Measurement of D. L. Driver Level

Driving level refers to the power used on the crystal oscillator, which is calculated by measuring the current (I) through the crystal oscillator, multiplied by the equivalent series resistance (ESR) of the crystal oscillator, the basic unit is μW. The formula is as follows：

$P(\mu W) = I^2 \times ESR$

In order to save power, it is generally required that the driving power is as low as possible. In addition, if the driving power is too high, the internal interface of the crystal oscillator will deteriorate, which will lead to the instability of the frequency oscillation and the attenuation of its life.

3. Measurement of negative impedance (-Rx, also known as excitation margin) :

Generally, the larger the negative impedance value, the better, indicating that the oscillating circuit is easier to start oscillation. If the negative impedance value is too low, the starting time will be longer, or even the phenomenon of no starting will occur. The normal negative impedance value must be 3 ~ 5 times of the maximum crystal oscillator ESR.

The following table is an actual test case:
MCU：PMS156 SO8
Crystal oscillator：YOKE AT-38 32.768KHz / 12.5pF / ±20ppm / 50Kohm / 1.0uW
The loop analysis results of the oscillating circuit are as follows:

Xtal No.	C1/C2 (pF)	F/on board (Hz)	F/on borad (ppm)	F/xtal (ppm)	On board Dev.(ppm)	ESR (ohm)	-Rx (ohm)	Drive Level (uW)
X1	22/22	32769636	49.93	12.98	36.95	13K	452K	< 1
X1	27/27	32768382	11.66	12.98	-1.32	13K	405K	< 1